> a first transistor for the logic device (110, Fig. 1) having a source (25, Fig. 1) and drain region (26, Fig. 1) includes a separated by a channel region (27, Fig. 1) in the substrate (21, Fig. 1) wherein the first transistor includes a dielectric layer (42, Fig. 3A) of a first thickness (Fig. 3A) including a top layer (43, Fig. 3A) which exhibits a high resistance to oxidation at high temperatures (1000°C), separating a gate (28, 29, Fig. 1) from the channel region (27, Fig. 1); and
>
> a second transistor for the memory device (210, Fig. 1) having a source (35, Fig. 1) and drain region (36, Fig. 1) in the substrate (21, Fig. 1) separated by a channel region (37, Fig. 1) in the substrate (21, Fig. 1) wherein the second transistor (210, Fig. 1) includes a dielectric layer (42, Fig. 3A) of a second thickness (fig. 3A) separating a gate (39,38, Fig. 1) from the channel region (37, Fig. 1) [col. 5, lines 37-42].

Okazawa appears to show forming "a thin silicon oxide film 42 and a silicon nitride film 43" (col. 5, lines 37-38). Okazawa also appears to show removing the silicon nitride film 43 and the silicon oxide film 42 and "newly" forming **gate oxide films 29, 39** (col 5, lines 43-45). However, Okazawa does not show, teach or suggest a dielectric layer of a first thickness, including a top layer which exhibits a high resistance to oxidation at high temperatures, separating a gate from the channel region. The gate oxides 29, 39 of Okazawa are formed after structures 42 and 43 have been removed. Because the structures 42 and 43 are temporary, and have been removed prior to forming a gate, Applicant respectfully submits that the structures 42 and 43 do not separate a gate from a channel region.

Further, Okazawa does not show a dielectric layer of second thickness separating a gate from the channel region. Applicant is unable to find any teaching or suggestion in Okazawa of forming gate oxides 29, 39, or any structures separating a gate from the channel region, at different thicknesses by any method.

Further, Okazawa does not show a logic device and a memory device structure on a single substrate. Applicant is unable to find any teaching or suggestion that structures in Okazawa are included in both a logic device and a memory device structure on a single substrate. In contrast, teachings of Applicant's present application overcome the technical hurdles and challenges of forming both a logic device and a memory device structure on a single substrate. One example of the technical hurdles and challenges involved is outlined on page 1, lines 20-24 where Applicant's specification states that "Efforts to merge DRAM and logic onto a single chip to

produce a "system on a chip" or other high function DRAM thus must confront the choice of either compromising the gate oxide thickness for one or both device types, or assume the complexity and expense of two separately grown gate oxides."

In contrast, Applicant's claim 33 includes a logic device and a memory device structure on a single substrate. Applicant's claim 33 further includes a dielectric layer of a first thickness, including a top layer which exhibits a high resistance to oxidation at high temperatures, separating a gate from the channel region. Applicant's claim 33 further includes a dielectric layer of a second thickness separating a gate from the channel region.

Because the Okazawa reference does not show every element of Applicant's independent claim 33, a 35 USC § 102(b) rejection is not supported. Reconsideration and withdrawal of the rejection is respectfully requested with respect to Applicant's independent claim 33. Additionally, reconsideration and withdrawal of the rejection is respectfully requested with respect to claim 34, that depends therefrom as depending on an allowable base claim.

§103 Rejection of the Claims

Numerous rejections under 35 USC § 103(a) were presented regarding claims 35-38, 40, 55-59, 61-70, 72, and 78-81. All of the 35 USC § 103(a) rejections combine Okazawa with additional references to form the rejection.

Applicant respectfully submits that none of the supporting references cure the deficiencies of Okazawa that have been outlined above in the 35 USC § 102(b) discussion.

Reconsideration and withdrawal of the 35 USC § 103(a) rejection is respectfully requested with respect to claims 35-38, 40, 55-59, 61-70, 72, and 78-81.

Allowable Subject Matter

Claims 73 - 77 and 82 - 86 were allowed. Applicant acknowledges and thanks the Examiner for allowance of these claims.

Claims 39, 60 and 71 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant acknowledges and thanks the Examiner for indicating allowability of claims 39, 60 and 71 if rewritten in independent form. However, as discussed above, applicant respectfully submits that independent claims 33, 55, 62, 67, 73, 78, 82, and 86 are in condition for allowance over the cited references.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612 373-6944) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

KIE Y. AHN ET AL.

By their Representatives,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 23rd day of July, 2002

Name Amy Moriarty Signature _____

Clean Version of Amended Specification Paragraphs

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES
Applicant: Kie Y. Ahn et al.
Serial No.: 09/943,324
Filed: August 30, 2001

The paragraph of the specification beginning on line 13 of page 12:

As can be understood from viewing Figure 2, a first transistor 201A formed in thin gate oxide region 212 for use in a logic device has a total dielectric layer of a first thickness, d1. Also as seen from viewing Figure 2 a second transistor 201B formed in the thick gate oxide region 214 for use in a memory device has a total dielectric layer of a second thickness, d2, which is greater than the dielectric layer of the first thickness, d1. The first transistor having a dielectric layer of a first thickness d1 includes a bottom layer 204A of silicon dioxide (SiO_2) and a top layer 206 of silicon nitride (Si_3N_4). The second transistor having a dielectric layer of a second thickness d2 includes a bottom layer 204B of silicon dioxide (SiO2) and an additional top layer 210 of silicon dioxide (SiO2). In one embodiment, the first transistor having a dielectric layer of a first thickness d1 includes a dielectric layer of a first thickness d1 which is less than 7 nanometers (nm). In this embodiment, the second transistor having a dielectric layer of a second thickness d2 includes a dielectric layer of a second thickness d2 which is less than 12 nm. In one embodiment, the first transistor having a dielectric layer of a first thickness d1 includes a dielectric layer of a first thickness d1 having a top layer 206 which exhibits a high resistance to oxidation at high temperatures. In one embodiment, the first transistor having a dielectric layer of a first thickness d1 has a top layer of silicon nitride (Si_3N_4) which comprises approximately a third of the first thickness d1 of the dielectric layer. In one embodiment, the first transistor 201A further includes a gate 220A, a first source/drain region 221A and a second source drain region 223A. In one embodiment, the second transistor 201B further includes a gate 220B, a first source/drain region 221B and a second source drain region 223B.